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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,464	09/08/2003	Masakatsu Uneme	N26532602E	9792

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/657,464	UNEME, MASAKATSU	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7,9-11 and 14-20* is/are rejected.

7)☒ Claim(s) *2 6 8 12 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 1-20 are presented for examination. This office action is in response to the amendment filed on 10/16/06.

Information Disclosure Statement

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Claim Objections

3. Claims 16, and 18-20 are objected to because of the following informalities:

As to claim 16 in line 2, it is unclear whether "data processing circuit" refers to "first data processing circuit" or "second data processing circuit". In line 11, it appears that "fist" should be changed to –first--.

As to claim 18 in line 5, it is unclear whether the data processing circuit refers to "first data processing circuit", "second data processing circuit" or " first or second data processing circuit".

As to claim 19 in line 3, it is unclear whether "data processing circuit" refers to "first data processing circuit" or "second data processing circuit".

As to claim 20 in line 3, it is unclear whether "data processing circuit" refers to "first data processing circuit" or "second data processing circuit".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Muramatsu et al. (Muramatsu) JP359183455.

As to claim 15, AAPA discloses a method of sharing a semiconductor memory circuit (Fig. 4 Ref. 100) with a plurality of data processing circuits (Fig. 4 Refs. 102s), comprises the steps of when a first data processing circuit (Fig. 4 Ref. 102) ends control of the semiconductor memory circuit, driving first control outputs connected to control lines for the semiconductor memory circuit to predetermined logic values (page 3 lines 10-14) and when a second data processing circuit (Fig. 4 Ref. 102) starts control of the semiconductor memory circuit, driving second control outputs connected to control lines to the predetermined logic values (Fig. 4 Ref. 10 and 106). However, AAPA does not specifically disclose subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state.

Muramatsu discloses subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit

that is ending control of the semiconductor memory circuit is placed in the high impedance state (constitution) for the purpose of access to a shared memory in time division.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state as taught by Muramatsu into the system of AAPA for the advantages stated above.

As to claim 16, AAPA and Muramatsu disclose the invention as claimed. Muramatsu further discloses the semiconductor memory circuit and data processing circuit operate in synchronism with a clock signal; when the first data processing circuit ends control of the semiconductor memory circuit, the first data processing circuit places the control outputs in the high impedance state a first number of clock cycles after ceasing operating with the semiconductor memory circuit; and when the second data processing circuit starts control of the semiconductor memory circuit, the second data processing circuit drives control outputs to the predetermined logic values a second number of clock cycles after the first data processing circuit that is ending control ceases operating with the semiconductor memory circuit; wherein the second number of clock cycles is less than the first number of clock cycles (constitution).

As to claim 17, AAPA and Muramatsu disclose the invention as claimed. Muramatsu further discloses the second number of clock cycles is one and the first number of clock cycles is two (constitution).

As to claim 9, AAPA discloses a data processing apparatus (Fig. 4), comprises a semiconductor memory circuit (Fig. 4 Ref. 101) that is controlled by control signal inputs to at least one control input (Fig. 4 Refs. 105 and 106); at least one control line coupled to the control input of the semiconductor memory circuit (Fig. 4 Refs. 105 and 106); and a plurality of data processing circuits (Fig. 4 Refs. 102s) that share access to the semiconductor memory circuit, each data processing having a control output coupled to the at least one control line and the data processing circuit provides a control signal at the control output at a predetermined potential and the another data processing circuit provides a control signal at its control output at the predetermined potential (page 3 lines 10-14).

However, AAPA does not specifically disclose wherein when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and subsequently when another data processing circuit starts control of the semiconductor memory circuit, the another data processing circuit provides a control signal at its control output at the predetermined potential within the first time period.

Muramatsu discloses wherein when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period (constitution) for the purpose of access to a shared memory in time division.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein when one data processing circuit ends control of the semiconductor memory circuit, the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and subsequently, when another data processing circuit starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period as taught by Muramatsu into the system of AAPA for the advantages stated above.

As to claim 14, AAPA and Muramatsu disclose the invention as claimed. Muramatsu further discloses the at least one control line is directly connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits (Fig. 1 and 2).

5. Claim s 1, 3, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Muramatsu et al. (Muramatsu) JP359183455 further in view of Wilcox et al. (Wilcox) U.S. Patent No. 6,510,099.

As to claim 10, AAPA and Muramatsu disclose the invention as claimed. However, neither AAPA nor Muramatsu disclose the semiconductor memory circuit operates in synchronism with a clock signal, and the at least one control input includes a chip select input that enables the processing of commands by the semiconductor memory circuit, and a clock enable signal that enables generation of timing signals within the semiconductor memory circuit.

Wilcox discloses the semiconductor memory circuit operates in synchronism with a clock signal, and the at least one control input includes a chip select input that enables the processing of commands by the semiconductor memory circuit, and a clock enable signal that enables generation of timing signals within the semiconductor memory circuit (col. 1 lines 32-40) for the purpose of synchronizing control signals.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the semiconductor memory circuit operates in synchronism with a clock signal, and the at least one control input includes a chip select input that enables the processing of commands by the semiconductor memory circuit, and a clock enable signal that enables generation of timing signals within the semiconductor memory circuit as taught by Wilcox into the combined invention of AAPA and Muramatsu for the advantages stated above.

As to claim 1, AAPA, Muramatsu, and Wilcox disclose the invention as claimed AAPA further discloses a data processing apparatus (Fig. 4) that arbitrates (Fig. 1 Ref. 103) sharing of a single semiconductor memory circuit (Fig. 4 Ref. 101) among multiple data processing circuits (Fig. 4 Refs. 102s), comprises a semiconductor memory circuit (Fig. 4 Ref. 101) that executes operations corresponding to a command signal, address signal and clock signal (page 2 lines 8-11) received external to the semiconductor memory circuit.

Muramatsu further discloses before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock at the same state as the first clock provided by the data processing circuit ending control of the semiconductor memory circuit (constitution).

Wilcox further discloses the semiconductor memory circuit includes a clock enable (col. 8 lines 22-24 and Fig. 5 Ref. CKE_1) signal input and a chip select signal input (col. 8 lines 20-22, Fig. 5 CS_1) and a data processing circuit that supplies the semiconductor memory circuit with a first clock enable signal output to the clock enable signal unit (col. 8 lines 22-24 and Fig. 5 Ref. CKE_1) for enabling an input of the clock signal when active and a disabling the input of the clock signal when inactive, and a first chip select signal output to the chip select signal input (col. 8 lines 20-22, Fig. 5 CS_1) for enabling input of command signals when the chip select signal is active and

disabling input of command signals when the chip select signal is inactive; wherein before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock enable signal output and first chip select signal output, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock enable signal output to the clock enable signal input and a second chip enable signal output to the chip enable signal input, the second clock enable signal output and the second chip enable signal output having clock enable signal and chip select signal logic values at the same state as the first clock enable signal output and the first chip enable signal output provided by the data processing circuit ending control of the semiconductor memory circuit for the purpose of supporting dynamic driver capability (col. 2 lines 3-5 and Fig. 5 Ref. CKE_2 and CS_2).

As to claim 3, AAPA, Muramatsu, and Wilcox disclose the invention as claimed. Wilcox further discloses the semiconductor memory circuit enters a lower power state when the clock enable signal is inactive, as compared to when the clock enable signal is active (col. 1 lines 32-40 and Low state of CKE).

As to claim 5, AAPA and Muramatsu disclose the invention as claimed. Muramatsu further discloses the multiple data processing circuits are connected to one another but formed independently of one another (Figs. 1 and 2).

6. Claims 11, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Muramatsu et al. (Muramatsu) JP359183455 further in view of Askinazi et al. (Askinazi) U.S. Patent No. 4,453,211.

As to claim 11, AAPA and Muramatsu disclose the invention as claimed above. However, neither AAPA nor Muramatsu specifically discloses a sharing arbitration circuit with request, busy, and grant signals.

Askinazi discloses a sharing arbitration circuit with request, busy, and grant signals (col. 7 lines 12-29) for the purpose of providing synchronous multi system operation.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a sharing arbitration circuit with request, busy, and grant signals as taught by Askinazi into the combined system of AAPA and Muramatsu for the advantages stated above.

As to claim 18, AAPA and Muramatsu disclose the invention as claimed above. However, neither AAPA nor Muramatsu specifically discloses a master and a slave devices.

Askinazi discloses a master and a slave devices (col. 7 lines 12-29) for the purpose of providing synchronous multi system operation.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a master and a slave devices as taught

by Askinazi into the combined system of AAPA and Muramatsu for the advantages stated above.

As to claim 19, AAPA, Muramatsu, and Askinazi disclose the invention as claimed above. Askinazi further discloses when the data processing circuit ends control of the semiconductor memory circuit; the data processing circuit sets a busy signal (col. 7 lines 12-29) to an inactive state.

As to claim 20, AAPA, Muramatsu, and Askinazi disclose the invention as claimed above. Askinazi further discloses when the data processing circuit seeks control of the semiconductor memory circuit; the data processing circuit activates a request signal (col. 7 lines 12-29).

7. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Muramatsu et al. (Muramatsu) JP359183455 and Wilcox et al. (Wilcox) U.S. Patent No. 6,510,099 further in view of Askinazi et al. (Askinazi) U.S. Patent No. 4,453,211.

As to claim 4, AAPA, Muramatsu, Wilcox and Askinazi disclose the invention as claimed above. However, neither AAPA, Muramatsu, nor Wilcox specifically discloses one of the multiple data processing circuits is a master device while any others are slave devices.

Askinazi discloses one of the multiple data processing circuits is a master device while any others are slave devices (col. 7 lines 12-29) for the purpose of providing synchronous multi system operation.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate one of the multiple data processing circuits is a master device while any others are slave devices as taught by Askinazi into the combined system of AAPA, Muramatsu and Wilcox for the advantages stated above.

As to claim 7, AAPA, Muramatsu, Wilcox, and Askinazi disclose the invention as claimed above. Askinazi further discloses each of the data processing circuits of the multiple data processing circuits includes a built in sharing arbitration circuit; the multiple data processing circuits are initialized to establish one data processing circuit as a master device and all others as slave devices; and the arbitration circuit of the master device is enabled and the arbitration circuits of the slave devices are disabled (col. 7 lines 12-29).

Allowable Subject Matter

8. Claims 2, 6, 8, 12, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcome claim objections.

Response to Arguments

9. Applicant's arguments filed on 10/16/06 have been fully considered but they are not persuasive.

Muramatsu discloses before the data processing circuit ends control of the semiconductor memory circuit and stops supplying the first clock, a different data processing circuit starting control of the semiconductor memory circuit supplies the semiconductor memory circuit with a second clock at the same state as the first clock provided by the data processing circuit ending control of the semiconductor memory circuit (constitution). Muramatsu also discloses subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state (constitution)

AAPA discloses two controller (Fig. 4 Refs. 109's). Muramatsu also discloses two controllers (Refs 9 and 10).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
December 12, 2006